

<b>Information Disclosure Statement</b>  <b>PTO - 1449</b>		Atty. Docket No: 60234 (45107)		Serial No. 10/719,818		
		Applicant(s): Stefan HÖRETH				
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<b>UNITED STATES PATENT DOCUMENTS</b>						
Exam. Initials	Ref. No.	Document Number	Date	Inventor(s)	Class	Filing Date
<b>FOREIGN PATENT DOCUMENTS</b>						
Exam. Initials	Ref. No.	Document Number	Date	Country or Office	Class	Translation
<b>OTHER DOCUMENTS (INCL. TITLE, AUTHOR, DATE, PAGES, ETC)</b>						
Exam. Initials	Ref. No.					
k	CA	Satyanarayana J.J. et al, "Systematic Analysis of Bounds on Power Consumption in Pipelined and Non-Pipelined Multipliers", IEEE Computer Society Press, October 7, 1996, pages 492-499.				
h	CB	Bobba S., et al. "Estimation of Maximum Switching Activity in Digital VLSI Circuits" IEEE August 3, 1997, pages 1130-1133.				
r	CC	Bhanja S., et al. "Switching Activity Estimation of Large Circuits Using Multiple Bayesian Networks", Proceedings of the 15 <sup>th</sup> International Conference on VLSI Design. IEEE Computer Society pages 187-192.				
Examiner: <i>Janaka</i>				Date: 6/9/05		